

AMENDMENTS TO THE CLAIMS

- 1 1. (Original) A memory system comprising:
 - 2 a plurality of memory devices coupled one to another in a chain;
 - 3 a memory controller coupled to the chain and configured to output a memory access
 - 4 command that is received by each of the memory devices in the chain and that selects
 - 5 a set of two or more of the memory devices to be accessed.

- 1 2. (Original) The memory system of claim 1 wherein the memory access command is a
2 memory read command that selects a set of the memory devices to be read by the memory
3 controller;

- 1 3. (Original) The memory system of claim 1 wherein the memory access command is a
2 memory write command that selects a set of the memory devices to store a sequence of
3 write data values.

- 1 4. (Original) The memory system of claim 1 wherein the set of memory devices
2 comprises fewer than all the memory devices in the chain.

- 1 5. (Original) The memory system of claim 1 wherein each of the memory devices in the
2 chain, except a last memory device, comprises an output port coupled to an input port of
3 another of the memory devices.

- 1 6. (Original) The memory system of claim 5 wherein a first memory device in the chain
2 comprises an input port coupled to the memory controller to receive the access command.

1 7. (Original) The memory system of claim 6 wherein the memory controller is coupled
2 to the input port of the first memory device in the chain via a point-to-point signaling path.

1 8. (Original) The memory system of claim 7 wherein the output port of each memory
2 device in the chain, except the last memory device, is coupled to the input port of one other
3 of the memory devices via a point-to-point signaling path.

1 9. (Original) The memory system of claim 5 wherein the last memory device comprises
2 an output port coupled to an input port of the memory controller.

1 10. (Original) The memory system of claim 1 wherein each of the memory devices in the
2 chain comprises an interface register having a buffer input and a buffer output, the buffer
3 output of each of the memory devices, except a last memory device in the chain, being
4 coupled to the buffer input of one other memory device in the chain via a respective point-
5 to-point signaling path.

1 11. (Original) The memory system of claim 10 wherein each of the memory devices in
2 the chain comprises a clock signal receiver coupled to receive a clock signal and having an
3 output coupled to a strobe input of the interface register.

1 12. (Original) The memory system of claim 11 wherein the interface register within each
2 of the memory devices is configured to store a value present at the buffer input in
3 synchronism with each rising edge transition of the clock signal.

1 13. (Original) The memory system of claim 12 wherein the interface register within each

2 of the memory devices is further configured to store a value present at the buffer input in
3 synchronism with each falling edge transition of the clock signal.

1 14. (Original) The memory system of claim 11 wherein the interface register within each
2 of the memory devices is configured to store a value present at the buffer input in
3 synchronism with each falling edge transition of the clock signal.

1 15. (Original) The memory system of claim 11 wherein each of the memory devices
2 further comprises a clock output driver having an input coupled to an output of the clock
3 receiver and output coupled to an input of the clock signal receiver within another one of
4 the memory devices.

1 16. (Original) The memory system of claim 10 wherein the interface register comprises a
2 first plurality of edge-triggered storage elements each having a strobe input coupled to
3 receive a clock signal.

1 17. (Original) The memory system of claim 16 wherein the interface register further
2 comprises a second plurality of edge-triggered storage elements each having a strobe input
3 coupled to receive a complement of the clock signal.

1 18. (Original) The memory system of claim 14 wherein each of the memory devices in
2 the chain further comprises an output data buffer and a select circuit, the select circuit
3 having a first input port coupled to the output data buffer, a second input port coupled to
4 the interface register and, in each of the memory devices in the chain except the last
5 memory device, an output port coupled to the buffer input of the interface register of the
6 one other memory device.

1 19. (Original) The memory system of claim 1 wherein each of the plurality of memory
2 devices is a discrete integrated circuit device.

1 20. (Original) The memory system of claim 1 further comprising a substrate and wherein
2 at least a portion of the memory devices are mounted to the substrate.

1 21. (Original) The memory system of claim 20 further comprising sets of conductive
2 traces formed on the substrate and coupled between respective pairs of the memory devices
3 mounted on the substrate.

1 22. (Original) The memory system of claim 1 further comprising a substrate having first
2 and second surfaces, and wherein a first portion of the memory devices are mounted on the
3 first surface of the substrate, and a second portion of the memory devices are mounted on
4 the second surface of the substrate.

1 23. (Original) The memory system of claim 22 further comprising:
2 a first sets of conductive traces coupled between respective pairs of the memory devices
3 mounted on the first surface of the substrate; and
4 a second sets of conductive traces coupled between respective pairs of the memory devices
5 mounted on the second surface of the substrate.

1 24. (Original) The memory system of claim 23 further comprising a set of conductive
2 traces extending from one of the memory devices mounted on the first surface to one of the
3 memory devices mounted on the second surface.

1 25. (Original) The memory system of claim 22 further comprising an interconnection
2 structure coupled to the memory controller, the substrate being removably coupled to the
3 interconnection structure.

1 26. (Original) A method of operation in a memory controller, the method comprising:
2 receiving a memory access request that specifies a range of memory addresses;
3 outputting a memory access command to a plurality of memory devices coupled one to
4 another in a chain, the memory access request including selection information, based
5 on the specified range of memory addresses, that selects a set of two or more of the
6 memory devices to be accessed.

1 27. (Original) The method of claim 26 wherein the memory devices in the chain are
2 associated with respective memory identifiers, and wherein the selection information
3 indicates at least two of the memory identifiers.

1 28. (Original) The method of claim 27 wherein each of the memory identifiers indicates
2 a position, within the chain, of the associated memory device, and wherein the selection
3 information comprises a start memory identifier and an end memory identifier that
4 collectively select all the memory devices disposed within the chain between the memory
5 devices associated with the start and end memory identifiers.

1 29. (Original) The method of claim 28 wherein the start memory identifier and end
2 memory identifier additionally select the two memory devices associated with the start and
3 end memory identifiers.

1 30. (Original) The method of claim 26 wherein the memory access request is a read
2 request and wherein the memory access command is a read command.

1 31. (Original) The method of claim 30 further comprising outputting a read-data pickup
2 command to the plurality of memory devices after outputting the memory access
3 command.

1 32. (Original) The method of claim 31 wherein outputting a read-data pickup command
2 comprises outputting a read-data pickup command that includes the selection information
3 that was included in the memory access command.

1 33. (Original) The method of claim 31 further comprising receiving read data from the
2 set of the memory devices selected by the selection information.

1 34. (Original) The method of claim 31 wherein outputting a read-data pickup command
2 after outputting the memory access command comprises delaying, after outputting the
3 memory access command, for a predetermined number of cycles of a clock signal before
4 outputting the read-data pickup command.

1 35. (Original) The method of claim 34 wherein delaying for the predetermined number
2 of cycles of the clock signal comprises retrieving a delay value indicative of the
3 predetermined number of cycles of the clock signal from a storage location within the
4 memory controller.

1 36. (Original) The method of claim 35 wherein retrieving the delay value from the

2 storage location comprises retrieving the delay value from one of a plurality of storage
3 locations within the memory controller according to the set of the memory devices to be
4 accessed.

1 37. (Original) The method of claim 36 further comprising reading parameter data from
2 each of the memory devices in the chain during a configuration operation, generating the
3 delay value based on the parameter data and storing the delay value in the one of the
4 plurality of storage locations.

1 38. (Original) The method of claim 26 wherein the memory access request is a write
2 request and wherein the memory access command is a write command.

1 39. (Original) The method of claim 38 further comprising:
2 receiving a plurality of write data values within the memory controller; and
3 outputting the plurality of write data values, one after another, to the plurality of memory
4 devices.

1 40. (Original) The method of claim 39 wherein outputting the plurality of write data
2 values to the plurality of memory devices comprises outputting the plurality of write data
3 values after outputting the write command.

1 41. (Original) The method of claim 40 wherein outputting the write command to the
2 plurality of memory devices comprises outputting the write command to a first memory
3 device in the chain via a point-to-point signaling path, and wherein outputting the plurality
4 of write data values after outputting the write command comprises outputting the plurality
5 of write data values, one after another, to the first memory device via the point-to-point

6 signaling path.

1 42. (Original) The method of claim 26 wherein outputting the memory access command
2 to the plurality of memory devices coupled in a chain comprises outputting the memory
3 access command to a first memory device in the chain, the first memory device being
4 configured to receive the memory access command and retransmit the memory access
5 command to a next-in-line memory device in the chain.

1 43. (Original) The method of claim 26 wherein receiving a memory access request that
2 specifies a range of memory address comprises receiving a memory access request that
3 specifies a starting address and a number of storage locations to be accessed.

Claims 44-77 (Cancelled)